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20	BRS	0	(back adj up) adj (scoreboard or (reservation adj station))	USPAT
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## SHADOW SCOREBOARD AND IMPLEMENTATION

Motorola's MC88100 processor is capable of concurrently processing multiple instructions at a single point of time if (1) the functional units processing each instruction is not full (there are multiple pipeline functional units: 3 stage integer processor, 5 stage floating point adder, 6 stage floating point multiplier) and if (2) the concurrently executing instructions are mutually independent - such that concurrent execution does not violate sequential program execution model.

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## SHADOW SCOREBOARD AND IMPLEMENTATION

by Yoav Talgam

Motorola's MC88100 processor is capable of concurrently processing multiple instructions at a single point of time if (1) the functional units processing each instruction is not full (there are multiple pipeline functional units: 3 stage integer processor, 5 stage floating point adder, 6 stage floating point multiplier) and if (2) the concurrently executing instructions are mutually independent - such that concurrent execution does not violate sequential program execution model.

The 88100 programming model is register based, i.e. all instruction operands originate and terminate in registers. Thus, the 88100 sequencer determines instruction dependencies through tagging the registers for being used as a destination of a yet incomplete instruction - withholding issuance of instructions as long as they declare a need to use such not-yet-ready operands or alter them as a result. This mechanism, which guarantees that concurrently executing instructions are independent, is called a scoreboard mechanism. It is implemented by keeping a single flag bit for each of the 32 88100 registers determining readiness. Logically, these 32 bit forms a control register - the processor scoreboard register.

In the 88100 many instructions can be outstanding when an internal exception or an external interrupt occurs. These outstanding instructions might correspond to many not-yet-ready registers, marked by their scoreboard flags. Logically, when context switching to the exception or interrupt handler context, no instructions of the current context may complete. Therefore, the processor scoreboard seen by the new context must indicate all ready. Tentatively, this could be accomplished by allowing all outstanding operations to complete prior to the context switch. This is useful in traps, where some of the outstanding instructions may be computing parameters for the operating system. In general, however, this is not desirable as some of the pipelines are of relatively long latencies and waiting for the whole machine to clear could result in high interrupt latency. Also, the outstanding instructions, if allowed to complete, might trigger further exceptions, which will necessitate additional complexity in the exception recovery logic.

The 88100 addresses this problem in a novel way: in addition to the processor scoreboard, a shadow scoreboard is implemented. During normal machine cycles, the shadow scoreboard follows (shadows) the processor scoreboard and the content of the processor scoreboard and the shadow scoreboard is identical. When an exception or interrupt is acknowledged by the machine, updates to the shadow scoreboard are immediately disabled. Thus, a copy of the processor scoreboard prior to when the machine enters exception

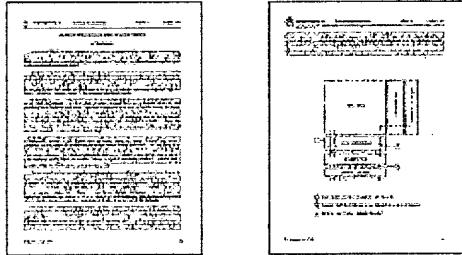
handling stage is kept in the shadow scoreboard. The processor scoreboard is then cleared, marking all machine resources as ava...

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**IPCOM #** 000005726D

**Published** 2001-10-31

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